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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/606,159	06/29/00	NAGAI T	037267/0135

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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED 01/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/606,159	NAGAI ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/124,851* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 21 recites the limitation "perpendicularly to word lines" in claims 21and 24 on line 10 on pages 23 and 24. There is insufficient antecedent basis for this limitation in the claims. For the purposes of this office action this limitation will not be given any patentable weight and will be ignored.

An additional limitation "extending in parallel with said word lines" occurs in claim 21 on line19 of page 23. There is insufficient antecedent basis for this limitation in the claims. For the purposes of this office action this limitation will not be given any patentable weight and will be ignored.

3. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "extended bit line" in claim 21 is used by the claim to mean "a stud or via connected to the drain region," while the accepted meaning is "a wire connecting drain regions together."

4. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "extended source line" in claim 24 is used by the claim to mean "a stud or via connected to the source region," while the accepted meaning is "a wire connecting source regions together."

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim.

Kamiya et al. discloses a method of fabricating an EEPROM semiconductor device in figures 1 – 7.

With regard to claim 21, Kamiya et al. discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel on a semiconductor substrate (100). Kamiya et al. discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya et al. then discloses in figure 1 forming a plurality of first polysilicon layers (107a) in parallel with one another. Kamiya et al. further discloses in figure 1 forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps. Kamiya et al. then discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon layer to thereby form a control gate (107) and a floating gate (107a). Kamiya et al. also discloses in figure 1 forming drain (109a) and source (109) regions. Kamiya et al. also discloses in figure 1 forming a first interlayer insulating layer (111) over the product resulting from the above steps. Kamiya et al. discloses in figure 4 forming a first metal wiring layer which is patterned so as to form both a common source line (114) connecting source regions to one another and an extended bit line (113) connecting the

drain region to a bit line. Kamiya et al. discloses in figures 6 and 7 forming a second metal wiring layer (118a) which is patterned so as to form a bit line connecting the drain regions to one another. Kamiya et al. does not disclose forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer. Kim teaches in figure 6 and column 3, lines 10 – 15 forming an interlayer insulating layer all over a product. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the interlayer insulating film of Kim in the process of forming a second metal wiring layer of Kimaya et al. in order to form a bit line as stated by Kim in column 3, lines 10 – 15.

With regard to claim 22, Kamiya et al. discloses in column 4, lines 46 – 51 that the second gate insulating film has a three-layer structure of oxide/nitride/oxide films.

With regard to claim 24, Kamiya et al. discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel on a semiconductor substrate (100). Kamiya et al. discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya et al. then discloses in figure 1 forming a plurality of first polysilicon layers (107a) in parallel with one another. Kamiya et al. further discloses in figure 1 that forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps. Kamiya et al. then discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon layer to thereby form a control gate (107) and a floating gate (107a). Kamiya et al. also discloses in figure 1 forming drain (109a) and source (109) regions. Kamiya et al. also discloses in figure 1 forming a first interlayer insulating layer (111) over the product resulting from the above steps. Kamiya et al. does not disclose forming a first metal wiring layer which is patterned so as to form both a bit line extending

almost in parallel with the field insulating films and connecting drain regions to one another, and an extended common source line connecting the source region to a latter mentioned common source line. Kamiya et al. does not disclose forming a second metal wiring layer which is patterned so as to form a common source line connecting the drain regions to one another. Kamiya et al. does not disclose forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer. Kim teaches in figure 8g and column6, lines 51 – 55 forming a first metal wiring layer which is patterned so as to form both a bit line 71 extending almost in parallel with field insulating films and connecting drain regions to one another, and an extended common source line (73) connecting the source region to a later mentioned common source line. While Kim describes the feature 71 as a source line, it is accepted in the art that a process used to make features of a source line can be interchanged with a process used to make a drain line as long as the opposite is true. Kim teaches in figure 6 and column 3, lines 10 – 15 forming an interlayer insulating layer all over a product. Kim teaches in figure 8g forming a second metal wiring layer (80) which is patterned so as to form a common source line connecting the drain regions to one another. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the wiring processes and interlayer insulating film of Kim in the fabrication of an EEPROM semiconductor device of Kimaya et al. in order to overcome the integration limitations caused by standard photolithography methods as stated by Kim in column 1, lines 52 – 60.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim. as applied to claim 21 above, and further in view of Yonemoto.

Kamiya et al. does disclose in column 5, lines 62 – 63 that the second wiring layers are composed of aluminum. Kamiya et al. does not disclose forming the first wiring layer of aluminum. Yonemoto does disclose forming a first wiring layer composed of aluminum in column 5, lines 8 – 11. It would have been obvious to use the aluminum wiring of Yonemoto in the process of Kamiya et al. in view of Kim in order to form signal lines to connect to the source region as stated by Yonemoto in column 5, lines 8 – 11.

8. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim. as applied to claim 24 above, and further in view of Cacharelis et al.

Kamiya et al. does not disclose forming backing wiring layers. Cacharelis et al. teaches in figure 20a forming backing wiring layers (490 and 500) connecting to a control gate at a certain interval and are constituted of a second metal wiring layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the backing wires of Cacharelis et al. in the method of Kamiya et al. in view of Kim in order to form a word lines as stated in column 5, lines 50 – 53.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mikata et al. discloses a method of forming a memory device. Chu, Sato, and Owens et al. disclose methods of forming and wiring memory devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 2, 2001

EDDIE C. LEE
PRIMARY EXAMINER